

ABSTRACT OF THE DISCLOSURE

A microprocessor for predicting a target address of a return instruction is disclosed. The microprocessor includes a BTAC and a return stack that each makes a prediction of the target address. Typically the return stack is more accurate. However, if the return stack mispredicts, update logic sets an override flag associated with the return instruction in the BTAC. The next time the return instruction is encountered, if the override flag is set, branch control logic branches the microprocessor to the BTAC prediction. Otherwise, the microprocessor branches to the return stack prediction. If the BTAC mispredicts, then the update logic clears the override flag. In one embodiment, the return stack predicts in response to decode of the return instruction. In another embodiment, the return stack predicts in response to the BTAC predicting the return instruction is present in an instruction cache line. Another embodiment includes a second, BTAC-based return stack.